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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,577	08/18/2003	Gregory J. Faanes	1376.711US1	3947
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH 1600 TCF TOWER 121 SOUTH EIGHT STREET MINNEAPOLIS, MN 55402			THOMAS, SHANE M	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/643,577	<b>Applicant(s)</b> FAANES ET AL.	
	<b>Examiner</b> Shane M. Thomas	<b>Art Unit</b> 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 1-6, 16-21 and 26-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7-15 and 22-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This Office action is responsive to the application filed 8/13/03. Claims 1-28 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as “[2/1-6].”

### ***Drawings***

The drawings are objected to under 37 CFR 1.84(m). The use of shading in views is encouraged if it aids in understanding the invention and if it does not reduce legibility. In the present case, the shading found in figures 4A, 4B, and 4C, does reduce legibility of the elements contained therein.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

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should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the Examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### *Election/Restrictions*

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-6 and 26, drawn to method and processing unit for executing memory instructions by creating a physical address and using the address to access either a local or remote cache, classified in class 711, subclasses 122 and/or 214.
- II. Claims 7-15 and 22-25, drawn to a method and a processor for storing memory requests into different queues based on whether or not the memory requests hit in the local cache, classified in class 711, subclass 118.
- III. Claims 16-21 and 27-28, drawn to a method and processing unit for synchronizing and caching scalar and vector memory instructions, classified in class 712, subclass 218.

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The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a method and processing unit for executing cache memory requests via a local or remote caching without having to necessarily update the local cache with a portion of the remote cache or separate memory requests into queues, as claimed by the method and processor unit of invention II. See MPEP § 806.05(d).

Inventions I and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a method and processing unit for executing cache memory requests via a local or remote cache without utilize a scalar or vector processor and a synchronization instruction to temporarily block particular memory access requests from executing. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II or Group III, restriction for examination purposes as indicated is proper.

During a telephone conversation with Thomas Brennan (Reg. No. 35,075) on 2/24/2006 a provisional election was made without traverse to prosecute the invention of Group II, claims

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7-15 and 22-25. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-6, 16-21, and 26-28 are withdrawn from further consideration by the Examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### *Specification*

The abstract of the disclosure is objected to because the abstract does not reflect the invention of Group II elected claims 7-15 and 22-25. Correction is required. See MPEP § 608.01(b).

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7-13, 22, and 23, are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes (U.S. Patent No. 6,393,536).

As per claim 7, Hughes teaches **obtaining a memory request [14/20-24], storing the memory request in a first memory request container (LS1 buffer 60 - [14/21-24]), and processing the memory request from the first memory request container by a cache controller (LS1 and LS2 control logic 64 and 66, respectively - [15/1-5]). The processing includes identifying a type of the memory request [16/17-18], processing the memory request in a local cache (data cache 28) as a function of a first condition (interpreted as fulfilling the memory request if it can be processed in the data cache 28 if the requested data is present (i.e. a “hit” in the data cache 28 - [16/61-17/20]), processing the memory request using a second memory request container (LS2 buffer 62) as a function of a second condition (during reprobing when the memory request misses the data cache 28 - [17/3-18/30]), and wherein the processing of the memory request using the second memory request container includes updating a portion of the local cache with a portion of a remote cache (L2 cache - [17/41-55]).**

As per claim 8, Hughes teaches **the obtaining of the memory request includes obtaining a memory load or a memory store request in [16/17-18].**

As per claim 9, Hughes teaches **wherein the storing of the memory request in the first memory request container (LS1 60) includes storing the memory request in an Initial Request Queue**, as the Examiner is considering the LS1 buffer to be an Initial Request Queue since all memory requests are initially stored there before probing (or accessing) the data cache 28 [14/20-24].

As per claim 10, as discussed above with respect to the rejection of claim 7, **the processing of the memory request in the local cache as a function of the first condition includes processing the memory request in the local cache when the local cache includes an entry associated with the memory request (i.e. the request hits the data cache 28) - [16/61-17/20]**.

As per claim 11, Hughes teaches **processing the memory request using a Forced Order Queue (FOQ) as a function of the second condition** since the Examiner is considering the LS2 buffer 62 to be a FOQ as requests are forced to execute there (i.e. by reprobing the local data cache 28 - [16/34-66] and [17/6-13]).

As per claim 12, Hughes teaches **processing the memory request as a function of the second condition includes processing the memory request using the FOQ when the memory request matches a corresponding request in the FOQ [18/11-30]**. Here, Hughes teaches that younger load requests can be fulfilled by older store requests when the address of the younger load and the older store coincide and the data for the older store is available. As a result of these *conditions*, data from the older store is forwarded to the younger load.

As per claim 13, Hughes teaches **adding the memory request to the FOQ when the memory request is not initially processed by the local cache (i.e. cache miss) and when the**

**memory request does not initially match a corresponding request already in the FOQ -** [18/24-30]. In order to match a corresponding request in the FOQ so that the memory request can be processed by the FOQ, a --match-- in the FOQ requires a pending FOQ entry to have (1) a coincident address with the incoming memory request and (2) available store data. Therefore, a memory request which is not initially processed by the local cache (a miss in data cache 28) and sent to the LS2 buffer (FOQ 62) and further does not --match-- a pending LS2 entry, is added to the FOQ as taught in the aforementioned passage, [18/24-30].

As per claim 22, Hughes teaches a **scalar processor** (figure 1) which **comprises a cache** (data cache 28), **a scalar load/store unit** (load/store unit 26) **having a first container** (LS1 60 - figure 3), **a second container** (LS2 62), **and a cache controller** (combination of control logic LS1 CTL 64 and LS2 CTL 66). The Examiner is considering the processor and the load/store unit to be --scalar-- elements as the elements perform calculations and memory operations, respectively, on scalar data (data items used to represent a single number). As can be seen, in [15/55-16/8], Hughes teaches that memory requests are the result of performing address calculations on data used to represent a single number (i.e. the address of the request for instance)). Further, Hughes teaches in [2/30-46] that the present invention is for use with *superscalar* processors.

Hughes further teaches **wherein the cache controller obtains a scalar load/store command from the first container, the scalar load/store command having a scalar load/store instruction and one or more addresses** [14/59-15/5], **the cache services the scalar load/store command when the scalar load/store command hits in the cache** [14/51-53], **the scalar load/store command is added to the second container when the scalar load/store**

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**command misses in the cache [14/24-27], and wherein one or more lines in the cache are allocated by a remote cache (L2 cache) when the scalar load/store command is added to the second container [17/41-55], as data is filled from the remote cache to the data cache 28 upon a miss.**

As per claim 23, Hughes teaches **the first container comprising an Initial Request Queue and the second container comprising a Forced Order Queue**, as discussed supra with respect to claim 9 (Initial Request Queue) and claim 11 (Forced Order Queue).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes (U.S. Patent No. 6,393,536) in view of Yamahata (U.S. Patent No. 5,247,639).

As per claim 14, Hughes teaches a multiprocessing system in figure 13 and [32/47-56] with processors 10 and 10a independently connected to the bus bridge 202 for connection to main memory 204. Hughes does not specifically teach **processing the memory request in the FOQ when local when local cache processing is bypassed**. Yamahata teaches a cache bypass bit for use when multiple processors are to obtain synchronization by using semaphore data in [2/4-38]. Specifically Yamahata teaches in [2/15-19] that an instruction decoder sends a bypass

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request to a bus control unit to bypass a local cache. Hughes shows a bus interface unit 37 connected to the load/store unit 26 in figure 2. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the multiprocessing system of Hughes with the cache bypassing during multiprocessor synchronization teaching of Yamahata in order to have been able to maintain a level of cache coherency between the processors 10 and 10a of modified Hughes when both processors would be attempting to update main memory 204. The utilization of semaphore data instructions are well known in the art to be utilized in multiprocessing systems for contention of a shared resource (in the case of Hughes, it would be main memory 204).

As per claim 15, the rejection follows the rejection of claim 14, *supra*. Local cache processing is bypassed when the memory request includes a synchronization request (i.e. via a cache bypass bit 801 - [7/23-35]). The memory request can be seen to be a **synchronization request** since the bypass bit would be set in a memory request when attempting to access semaphore data to attain synchronization between the multiple processor 10 and 10a of modified Hughes 10 and 10a [2/35-38 Yamahata.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes (U.S. Patent No. 6,393,536).

As per claim 24, Hughes teaches that in one specific implementation of the present embodiment of the invention, the data cache 28 comprises an **address generator** (address translation circuitry) **to generate one or more physical addresses from the one or more addresses of the scalar load/store command** [17/20/23]; however, Hughes does not specifically

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teach the address generator being a part of load/store unit 26. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the load/store unit 26 of Hughes by implementing the address translation circuitry as part of the load/store unit 26 instead of the data cache, since it has been held that rearranging parts of an invention involves only routine skill in the art. Refer to MPEP § 2144.04(vi). Such a modification would have increased the speed in which translated addresses are written into the LS2 buffer by not having to send the translated physical address across the address bus 80 [17/34-37].

As per claim 25, Hughes teaches **wherein the address generator** (address translation circuitry) **generates the one or more physical addresses using a translation look-aside buffer (TLB)** [17/27-31].

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hennessy et al. shows in figure 7.25 on page 593 that the TLB and the Cache, while inter-related, are nonetheless distinct entities.

IEEE 100 teaches on page 1003 the [computer] definition of --scalar--.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The Examiner can normally be reached M-F 8:30 - 5:30.

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If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shane M. Thomas



**HONG CHONG KIM**  
**PRIMARY EXAMINER**